

Notice of References Cited

Application/Control No.

10/786,276

Applicant(s)/Patent Under
Reexamination
MASLEID ET AL.

Examiner

Craig A. Thompson

Art Unit

2813

Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,895,487	04-1999	Boyd et al.	711/122
*	B	US-6,397,324	05-2002	Barry et al.	712/225
*	C	US-6,381,669	04-2002	Chudnovsky et al.	711/5
*	D	US-4,538,247	08-1985	Venkateswaran, Kalyanasundaram	365/230.06
*	E	US-5,956,597	09-1999	Furukawa et al.	438/405
*	F	US-5,894,152	04-1999	Jaso et al.	257/347
*	G	US-5,612,246	03-1997	Ahn, Jong-Hyon	438/405
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Rudack et al. "Yield Enhancement Considerations for a Single-Chip Multiprocessor System with Embedded DRAM" International Symposium on Defect and Fault Tolerance in VLSI Systems, November 1-3, 1999. IEEE, pp.31-39.
	V	Crowder, S. et al. "An Embedded DRAM High Performance 0.18 um Logiv Technology with Copper Beol" 1998 Int'l Electron Devices Meeting. Technical Digest. 12/6-9/98.
	W	Bernstein, K. et al. "SOI Circuit Design Concepts. Kluwer Acadmic Publishers, 2000. TK7871.99.M44B48 2000.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.